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Research Article

Low-Frequency Noise Related to the Scattering Effect in p-Type Copper(I) Oxide Thin-Film Transistors

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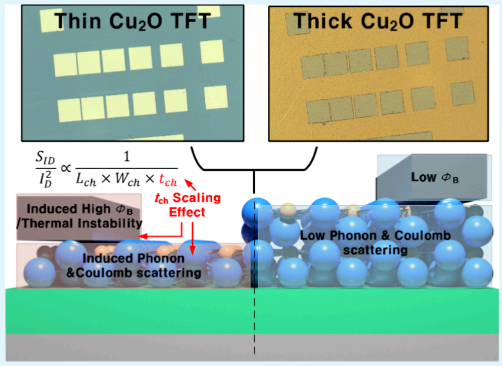
ABSTRACT: In this study, we investigate the origins of low-frequency noise (LFN) and $1/f$ noise in Cu_2O thin-film transistors (TFTs). The static direct current (DC) $I-V$ characterization demonstrates that the channel resistance (R_{ch}) contributes significantly to mobility degradation in the TFTs, with channel thickness (t_{ch}) controlled through the plasma-enhanced atomic layer deposition (PEALD) process. The $1/f$ noise followed the Hooge mobility fluctuation (HMF) model, and it was observed that both Coulomb and phonon scattering within the channel, which increased with a decrease in t_{ch}, contributed simultaneously. Increased R_{ch} contributed more significantly to the $1/f$ noise than to the contact resistance (R_C), as evidenced by the R_C configuration of the measurements, which also revealed that R_C depends upon t_{ch}. This study demonstrates that t_{ch} is a major noise source in Cu_2O TFTs and presents guidelines for the development of Cu_2O TFTs and potential high-mobility p-type oxide semiconductors.



KEYWORDS: *copper(I) oxide semiconductor, low-frequency noise, Hooge mobility fluctuation, transmission line method (TLM), channel resistance, scattering, Arrhenius plot*

INTRODUCTION

The valence band (VB) of oxide semiconductors (OS) is defined by a flat and localized O 2p-derived feature at the top and a deep valence band maximum. It results in holes being effectively trapped by defects such as oxygen vacancies with relatively low energy, thereby leading to a severe bottleneck in hole mobility (μ_h).[1−4] Unlike the VB, the conduction band (CB) of the OS typically comprises empty ns orbitals ($n \geq 4$) of the heavy post-transition metal. Therefore, high electron mobility is expressed even in the amorphous phase and provides accessibility to high on/off current control.[5−9] Copper(I) oxide (Cu_2O), a p-type oxide semiconductor, contains an intrinsic orbit from the close energy levels of the Cu 3d and O 2p orbitals. In high-quality single-crystal Cu_2O, the controllable hole concentration (n_h) of 10^9−10^{12} cm^{-3} contributes significantly to achieving high μ_h, exceeding >100 cm^2 V^{-1} s^{-1}.[5−14] However, when Cu_2O is fabricated as a thin-film transistor (TFT), there is a significant decrease in the carrier transport properties, which is attributed to the impact of the Schottky contact resistance (R_C) and the disordered quality of the semiconductor/oxide interface.[15−19]

The power spectral density (PSD) represents the correlation between signal power and frequency. That can be improved based on the low-frequency noise (LFN) measurement time, which is inefficient for achieving high system accuracy because it increases the measurement time in digital electronic devices. It is essential to understand the random fluctuations occurring at low frequencies for application in electronic devices and integrated circuits.[20−23] Therefore, LFN is appropriate for analyzing the charge transport mechanisms because it is always present in electronic materials and devices at the nanoscale as a determining component for the signal lower limit of both analog and digital integrated circuits. Typically, the flicker noise ($1/f$) is considered in the frequency range of less than several kilohertz (kHz). The $1/f$ noise is represented by the Hooge mobility fluctuation (HMF) of the Hooge model when current fluctuations occur owing to phonon scattering or impurity scattering and the charge number fluctuation (CNF) of the McWhorter model when the current fluctuates due to the trapping/detrapping effect of the carrier between the gate oxide and channels.[24−28] However, because the CNF model was originally based on single-crystal Si-based field-effect transistors, attempts have been made to interpret the OS with opposite conduction mechanisms as models reflecting the HMF and R_C.[22,23]

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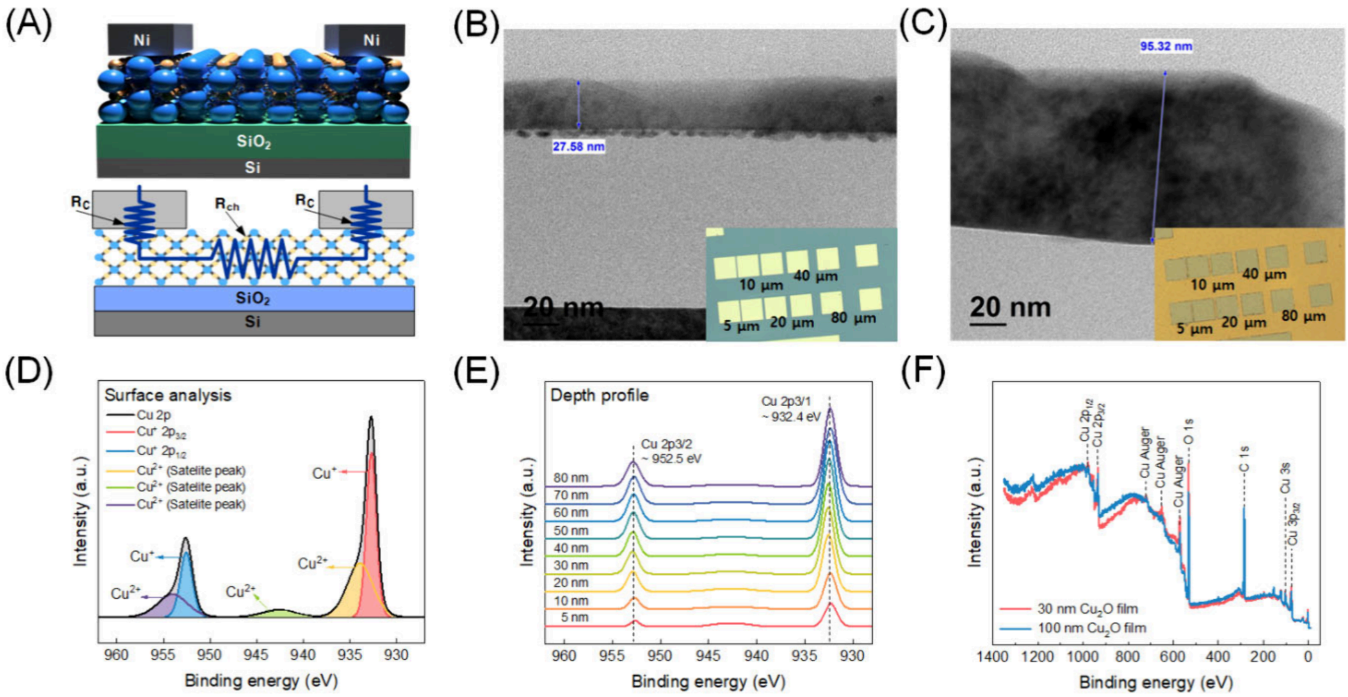

Figure 1. (A) Three-dimensional structure of Cu_2O TFT and the resistance model manufactured in this study. (B and C) TEM images of approximately 30 nm (1200 cycles) and 100 nm (3600 cycles) Cu_2O thin films deposited through the PEALD process and OM images of 30 and 100 nm Cu_2O TFTs with inserted TLM patterns. (D) High-resolution photoelectron spectrum on the Cu 2p binding energy region of the PEALD Cu_2O thin-film surface. (E) XPS depth profile of the Cu 2p binding energy region of the PEALD Cu_2O thin film. (F) Wide scan energy spectrum of 30 and 100 nm Cu_2O thin films.

In this article, we investigate the low-frequency noise in Cu_2O TFTs for the first time and discuss the mechanism of their mobility degradation. Our results are interpreted in terms of the HMF model, which is generally used for mobility analysis in p-type semiconductors.[29] The scattering-related noise is observed to increase throughout the channel due to impurity-dependent Coulomb scattering and phonon scattering by the lattice vibration as the thickness (t_{ch}) scales down. The channel and contact noise were found to depend upon the length (L_{ch}), width (W_{ch}), and t_{ch}, which are components of the OS channels. The reduction in the mobility of Cu_2O TFTs with controlled t_{ch} through the plasma-enhanced atomic layer deposition (PEALD) process was investigated via various electrical analyses, along with LFN. The parameters affecting the mobility, such as R_C, channel resistance (R_{ch}), temperature function, and surface roughness of the Cu_2O TFTs, were comprehensively investigated. Furthermore, this study revealed that the degradation in mobility decreased significantly with a decrease in t_{ch}. This suggests that the mobility degradation of the Cu_2O TFTs can be attributed to the Schottky contacts and interfaces, as reported in previous studies, and to the entire Cu_2O TFT structure.

RESULTS AND DISCUSSION

Figure 1A depicts the three-dimensional (3D) structure of the Cu_2O TFT fabricated in this study and the defined R_C and R_{ch}. The Cu_2O thin film was deposited in 1200, 1600, and 3600 cycles through the PEALD process to adjust the thickness. The detailed device fabrication process is presented in the Experimental Methods.[30,31] Panels B and C of Figure 1 show the transmission electron microscopy (TEM) cross-sectional images of the Cu_2O TFT. The Cu_2O deposited with 1200 cycles and 3600 cycles was found to have a thickness of approximately 30 and 100 nm, respectively, and the color of the thin film changed from blue to yellow as the thickness increased through the insertion image. Figure S1 of the Supporting Information presents the TEM images captured at 100 nm intervals, including the 40 nm Cu_2O thin film deposited at 1600 cycles. The transmission line method (TLM) pattern with L_{ch} of 5, 10, 20, 40, and 80 μm was formed as an electrode with a size of 100 × 100 μm^2, which can be confirmed in the inserted optical microscopy (OM) images presented in panels B and C of Figure 1. The chemical composition of the Cu_2O thin film was characterized using energy-dispersive X-ray spectroscopy (EDS) in scanning transmission electron microscopy (STEM) mode, as shown in Figure S2 of the Supporting Information. Cu was strongly detected in a relatively thick 100 nm Cu_2O thin film, indicating an uneven distribution in which Cu appeared to be short-circuited in some of the measurement areas. The time-of-flight secondary ion mass spectrometry (ToF-SIMS) analysis in Figure S3 of the Supporting Information shows a thickness contrast exceeding 3-fold, resembling the thickness variation observed in the TEM image comparison. The roughness of the Cu_2O TFT was significantly increased during postdeposition annealing (PDA) employing through the PEALD process to achieve a uniform ultrathin film, as shown in the TEM image and the atomic force microscopy (AFM) image in Figure S4 of the Supporting Information.[32−34] Based on previous research results on Cu_2O TFTs, it was noted that the particle size increased by approximately 8 times during PDA in a vacuum atmosphere, and the particle structure merged with the increase in temperature during PDA, but this induced the formation of the Cu_2O phase.[11,32,33] The high surface roughness of the Cu_2O thin film contributed to the formation of a non-uniform electrode, but it was deposited cleanly

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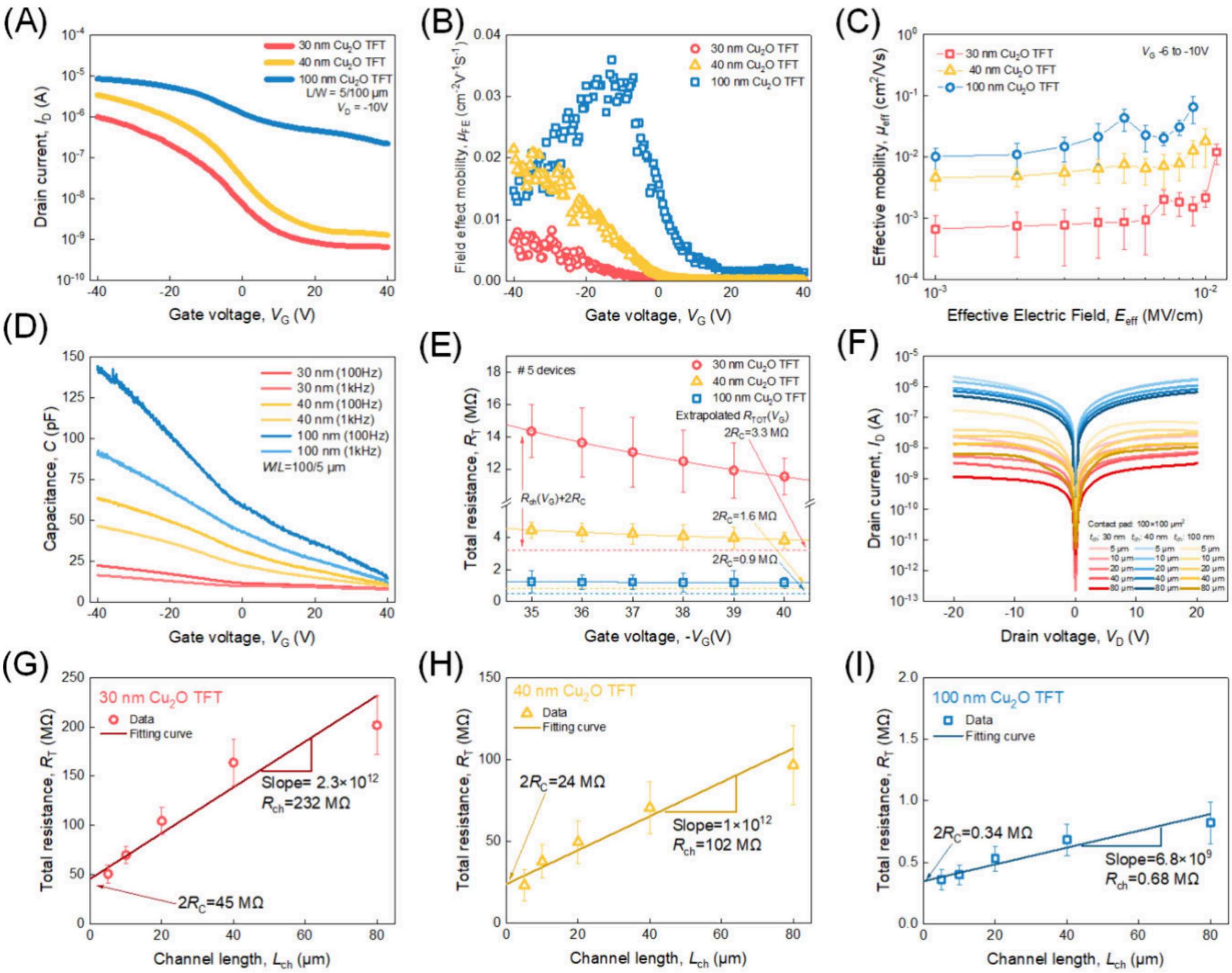

Figure 2. (A–D) Transfer, μ_{FE}, μ_{eff}, and capacitance density characteristics of 30, 40, and 100 nm Cu_2O TFTs, respectively. (E) Extracted R_{ch} and R_C as a function of V_G in the fabricated Cu_2O TFTs with various t_{ch} (30, 40, and 100 nm) by CRM method. (F) I–V characteristics of 30, 40, and 100 nm Cu_2O TFTs for TLM at room temperature. (G–I) Extracted R_{ch} and R_C in the fabricated Cu_2O TFT with various t_{ch} (30, 40, and 100 nm) by TLM method from the TLM pattern of panel C, respectively.

without gap at the metal–semiconductor junction and the related TEM image can be confirmed in Figure S5 of the Supporting Information. Panels D–F of Figure 1 depict the surface, depth profiling, and wide scan energy spectrum of Cu_2O TFTs analyzed through X-ray photoelectron spectroscopy (XPS), respectively, where the peak fitting of the Cu^+ peak indicates the formation of Cu_2O thin films.[10,35,36] However, the presence of some parasitic Cu^{2+} peaks in Figure 1D indicates that in some Cu_2O lattices, oxygen is combined with copper, leading to a thermodynamic transformation to CuO. The band gaps of Cu_2O and CuO are 2.0–2.2 and 1.2–1.7 eV, respectively, so oxidation from Cu_2O to CuO can lead to increased leakage current, potentially lowering the current on–off ratio. Additionally, the mobility degradation of Cu_2O TFTs is inherently affected by the higher effective mass associated with CuO formation.[10] Figure 1E shows that this transformation is a non-consideration since it moves away from the surface. Furthermore, we employed Ni electrodes to effectively reduce the Schottky barrier of the Cu_2O films based on the findings of previous studies.[16] Figure S6 of the Supporting Information presents the ultraviolet photoelectron spectroscopy (UPS) spectrum. It is assumed that the mobility degradation of the Cu_2O TFT in R_{ch} is severely reduced through the low Schottky barrier of Cu_2O and Ni junctions.

Figure 2A shows the transfer characteristics of the Cu_2O TFTs with a 5 μm channel and thickness of 30, 40, and 100 nm, demonstrating that the on–off current is effectively controlled in the 30 nm thick TFT when compared to the 100 nm thick TFT.[37] Figure S7 of the Supporting Information depicts the transfer, and output characteristics of the 30, 40, and 100 nm Cu_2O TFTs in different voltage ranges. Figure 2B presents a comparison of the field-effect mobility (μ_{FE}) characteristics estimated from the transconductance (g_m). Consequently, the 30 nm Cu_2O TFT lower mobility than the 100 nm Cu_2O TFT, which can be expected to degrade the mobility with the t_{ch} of the Cu_2O TFT. Figure 2C presents the effective mobility (μ_{eff}) corresponding to the t_{ch}, which indicates that the resistance effect caused by the thickness variations must be carefully examined as a main contributing component to the mobility degradation in Cu_2O TFT.[38] Conversely, the hall mobility of the epitaxially grown Cu_2O thin films known as high mobility p-type semiconductors, was

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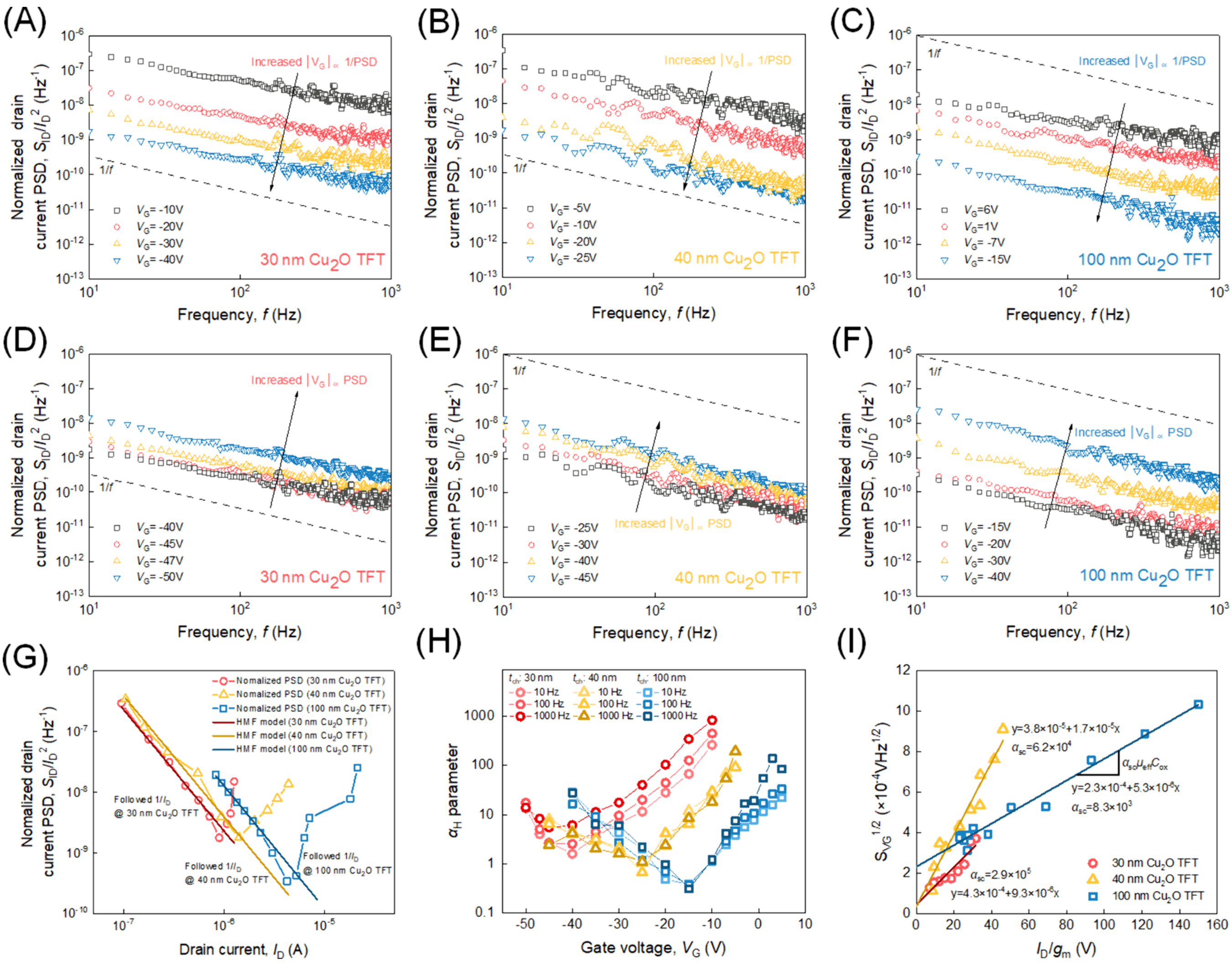

Figure 3. (A and D) S_{I_D}/I_D^2 compared to the frequency of 30 nm Cu_2O TFT; S_{I_D}/I_D^2 increase occurs from −40 V. (B and E) S_{I_D}/I_D^2 compared to the frequency of 40 nm Cu_2O TFT; S_{I_D}/I_D^2 increase occurs from −25 V. (C and F) S_{I_D}/I_D^2 compared to the frequency of 100 nm Cu_2O TFT; S_{I_D}/I_D^2 increase occurs from −15 V. (G) S_{I_D}/I_D^2 compared to the drain current of the 30, 40, and 100 nm Cu_2O TFT; S_{I_D}/I_D^2 follows the HMF model in the linear region and increases due to the resistance effect when it reaches the saturation region. (H) α_H corresponds to V_G. (I) Comparison of Coulomb scattering effects through the extraction of α_{sc}.

estimated to decrease rapidly due to the Fermi level pinning or trap states in the channel and/or interface.[11] Figure 2D presents the capacitance density of Cu_2O TFT compared to the V_G value measured at frequencies of 100 and 1000 Hz, and the amount of charge that is proportionally accumulated decreases as t_{ch} decreases.

To characterize the resistance effect corresponding to Cu_2O thin-film thickness, we implemented the channel resistance method (CRM) based on the gate bias and the TLM excluding the gate bias influence.[39−45] Figure 2E compares the resistance obtained through the CRM method, and the R_C of 30 nm Cu_2O TFT increased by approximately 4 times the R_C value when compared to that of the 100 nm Cu_2O TFT.[39−41] Figure 2F presents the $I-V$ measurement of the Cu_2O TFT with t_{ch} of 30, 40, and 100 nm, confirming the formation of a low Schottky barrier in the Cu_2O TFT due to the Ni electrodes, as mentioned above.[16] Panels G−I of Figure 2 depict the respective total resistances (R_T) separated through the TLM pattern, which can be obtained as $R_T = 2R_{metal} + 2R_C + R_{ch}$.[42−44] R_C and R_{ch} can be extracted through linear fitting by analyzing the slope of the linear region, with R_{metal} being negligible. The resistance estimated through the CRM and TLM methods was observed to increase rapidly with the decrease in t_{ch} in the Cu_2O TFT (based on the 30 nm Cu_2O TFT when compared to the 100 nm Cu_2O TFT by TLM the method: R_C = approximately 130 times, R_{ch} = approximately 340 times).

The identified R_C and R_{ch} values indicate a clear potential for shorter channel lengths and lower thicknesses to be significant factors in further reducing μ_{eff}. Panels A−F of Figure 3 show the representative normalized drain current spectral density (S_{I_D}/I_D^2) versus frequency characteristics of the Cu_2O TFTs for channel thicknesses of 30, 40, and 100 nm, respectively. The I_D dependence of S_{I_D} in panels A−F of Figure 3 can be found in Figure S8 of the Supporting Information. The results were measured by sequentially increasing the gate bias of the Cu_2O TFT in a linear region (V_D = −10 V) and were normalized to the sensitivity and drain current values through the direct current (DC) $I-V$ measurement. S_{I_D}/I_D^2 decreased

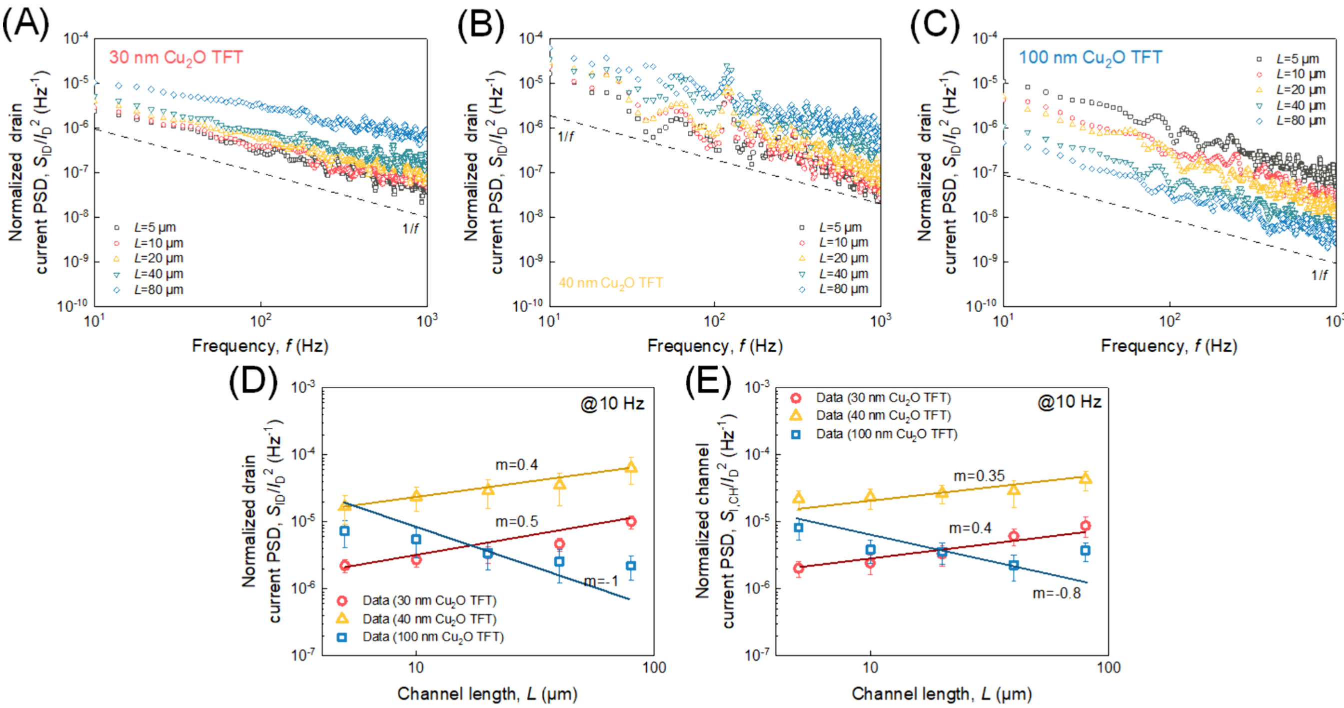

Figure 4. (A−C) S_{I_D}/I_D^2 compared to the frequency of 30, 40, and 100 nm Cu_2O TFTs measured under the same conditions for each L_{ch} through TLM pattern. (D) L_{ch} versus S_{I_D}/I_D^2. (E) Noise origin of the Cu_2O TFT closely correlates to the channel compared to $S_{I,ch}/I_D^2$ shown in panel D, when compared to the L_{ch} defined by eq 4.

as $|V_G|$ increased (panels A−C of Figure 3) but increased inversely when a specific $|V_G|$ was applied. The turn-up in S_{I_D}/I_D^2 occurs when significant contact noise (S_{R_C}) prevails over the channel resistance noise ($S_{R_{ch}}$) at a high drain current.[27,46] In panels D−F of Figure 3, the resistance-related noise increases only with a small gate bias in the 100 nm Cu_2O TFT when compared to the 30 nm Cu_2O TFT. This result indicates that the intrinsic R_{ch} of the 30 nm Cu_2O TFT is directly involved in the reduced mobility compared to R_{ch} of a 100 nm Cu_2O TFT. Figure 3G shows the concurrence between the HMF model, expressed as $1/I_D$, and the noise properties of the Cu_2O TFT accounting for the noise properties in the subthreshold region. This indicates that the physical noise of the Cu_2O TFT corresponds to phonon lattice scattering of holes within the bulk. The HMF model causes random mobility fluctuations, as follows:

$$\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H q}{f C_{ox} W L (V_G - V_T)} \quad (1)$$

where f is the frequency, C_{ox} is denotes the gate oxide capacitance per unit area, q is the electron charge, and W and L are the channel length and width, respectively. The Hooge parameter (α_H) is commonly used as a performance index for comparing various device technologies and its numerical value is proportional to that when phonon lattice scattering occurs strongly.[25,28] Figure S9 of the Supporting Information, presents a comparison with the CNF model, which is the carrier trapping/detrapping effect from the Cu_2O TFT to the gate oxide. S_{I_D}/I_D^2 demonstrated a significant difference from the trend of $(g_m/I_D)^2$, which indicates that the charge transport mechanism of the Cu_2O TFT follows the HMF model.

Figure S10A of the Supporting Information depicts the relationship between γ and V_G, which is the slope of the algebraic relationship between S_{I_D} and f of the Cu_2O TFT [$\gamma = -\partial \ln(S_{I_D})/\partial \ln(f)$]. The slope becomes smaller if parasitic noise other than the $1/f$ noise is affected. Thus, a decrease in the t_{ch} value induces a parasitic resistance effect; thus, a reduction in the thickness of the Cu_2O TFT is considered an additional noise source. In Figure 3H, the α_H extracted from the HMF model is significantly higher than the commonly known value $(10^{-4}–10^{-6})$.[47] Based on the fatally high roughness and its nature as a p-type semiconductor, α_H of Cu_2O TFT is considered a sufficiently probable value. Table S1 of the Supporting Information presents the α_H values of p/n-type semiconductors, and the α_H value of the Cu_2O TFT reported in this paper is similar to that of the reported p-type semiconductor. α_H decreases when the gate bias increases in the weak inversion region. The degradation persisted up to the peak voltage of g_m because the transfer properties influenced the lattice-related scattering effect more proactively. The R_C effect becomes more prominent with a further increase in the gate bias, leading to an increase in the α_H. Figure 3I gives the Coulomb scattering parameter (α_{sc}) extracted from the S_{I_D}/I_D^2 of the equivalent gate voltage noise (S_{VG}).[48,49] α_{sc} is valid only for FETs with bulk channels. α_{sc} recorded values nearly 30 times higher in 30 nm Cu_2O TFTs than in 100 nm Cu_2O TFTs, indicating that the scattering effects by the impurities are latent despite the low thickness. Strong Coulomb scattering effects on the LFN properties can be partly attributed to unwanted external noise sources presented by R_C or the electrical barrier height.[50−52] The μ_{eff} determined in Figure 2B is derived from the mobility by Coulomb scattering and phonon scattering, based on Matthiessen's rule. Therefore, due to the thickness reduction of the Cu_2O TFT, μ_{eff} is reasonably

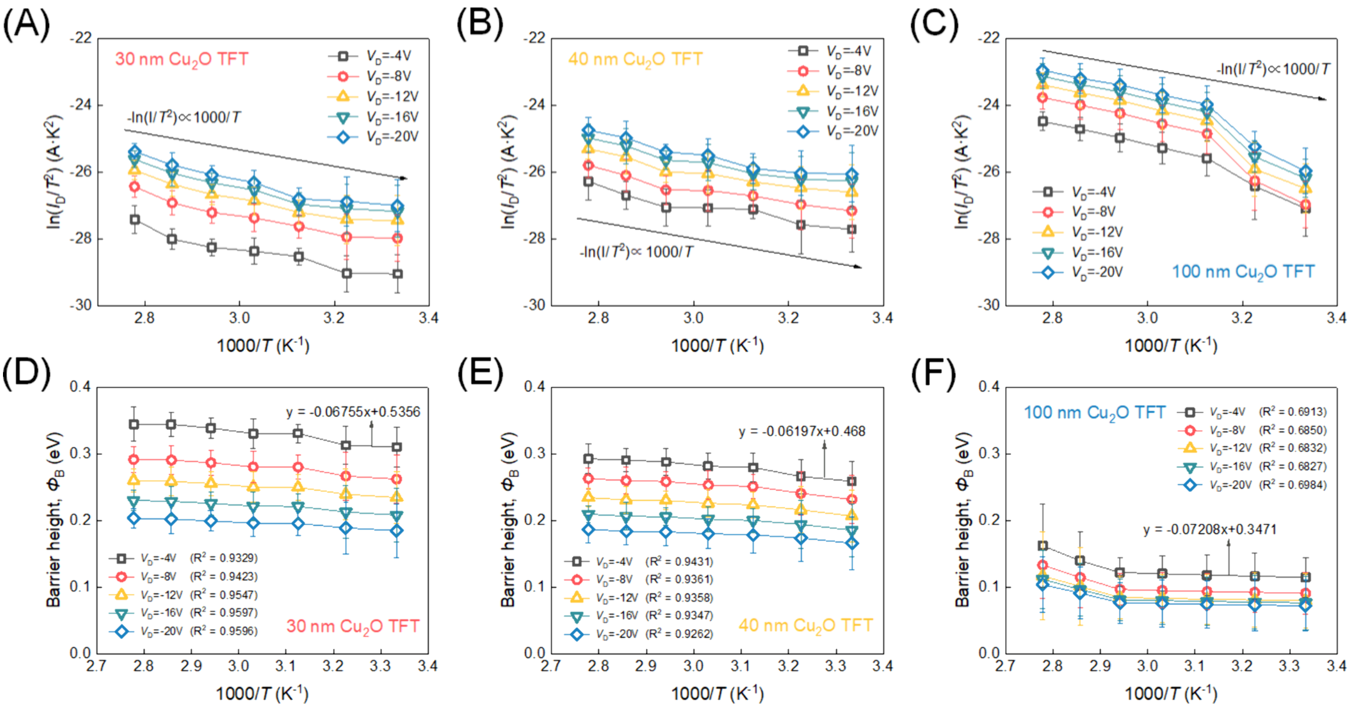

Figure 5. (A–C) Richardson plot compared to the temperature of a 30, 40, and 100 nm Cu_2O TFT with a 5 μm channel. (D–F) Temperature versus Φ_B defined through the Arrhenius plot. The legend includes the R^2 value for linear fit accuracy, along with the linear equation for $V_D = -4$ V.

assumed to be limited to the two scattering effects analyzed from the LFN characteristics of panels G and H of Figure 3. The following assumptions can be emphasized for Cu_2O TFTs with Ti electrodes that maximize Schottky barrier effects and are discussed in detail in Figure S11 of the Supporting Information. The error bars in panels B and C of Figure S10 of the Supporting Information depict a comparison of the scattering parameters of several devices.

It was observed in Figures 2 and 3 that R_{ch} is more involved than R_C as a major μ_{eff} degradation mechanism for the Cu_2O TFTs.[53] By utilizing the characteristic that R_C was proportional to W_{ch} and not dependent upon L_{ch}, we focused only on the effects of R_{ch} by maintaining W_{ch} at a constant value and varying L_{ch} to analyze the mobility degradation mechanism.[22] Panels A–C of Figure 4 show the S_{I_D}/I_D^2 results of the 30, 40, and 100 nm Cu_2O TFTs whose L_{ch} was increased 2 times from 5 μm through the TLM pattern. The S_{I_D}/I_D^2 comparison was performed under the condition of a gate/drain bias (−10/−10 V), which is the linear region of all devices, indicating that both the elements constituting the channel (L_{ch}, W_{ch}) and the applied voltage are identical except for the channel thickness. Notably, panels A–C of Figure 4 depict opposite S_{I_D}/I_D^2 movements, suggesting that t_{ch} of the Cu_2O TFT influenced $1/f$. To verify this trend, S_{I_D}/I_D^2 was assumed to be the total resistance noise (S_{R_T}) caused by uncorrelated R_{ch} and R_C based on the following equation:

$$\frac{S_{I_D}}{{I_D}^2} = \frac{S_{R_T}}{{R_T}^2} = \frac{S_{R_{ch}} + S_{R_C}}{(R_{ch} + R_C)^2} \tag{2}$$

In a previous study analyzing the LFN of nanocrystal field-effect transistors, four components ($S_{R_{ch}}$, S_{R_C}, R_{ch}, and R_C) were reported on the W_{ch}- and L_{ch}-dependent noise of the channel.[22] However, in the case of metal oxide semiconductors such as Cu_2O TFTs, the t_{ch} effect must be reflected because the bulk channel participates in current conduction. Figure S12 of the Supporting Information presents the ratio of R_C and R_{ch} to R_T extracted from DC I–V in the linear region by applying a gate bias of −10 V. In comparison, the R_C ratio at this voltage decreased as L_{ch} increased. Both R_{ch} and $S_{R_{ch}}$ significantly affect the $1/f$ shape when compared to R_C and S_{R_C} and are expressed as follows:

$$\frac{S_{I_D}}{{I_D}^2} = \frac{S_{R_T}}{{R_T}^2} = \frac{S_{R_{ch}}}{{R_{ch}}^2} \propto \frac{\frac{\alpha_{ch} {R_{ch}}^2}{N_{ch} f}}{{R_{ch}}^2} \propto \frac{1}{N_{ch}} = \frac{1}{L_{ch} \times W_{ch} \times t_{ch}} \tag{3}$$

where N_{ch} denotes the free carriers in the channel region. It corresponds to L_{ch}, W_{ch}, and t_{ch}, and can be simplified as $N_{ch} \propto L_c \times W_{ch} \times t_{ch}$. Meanwhile, R_{ch} has a proportional relationship with $L_{ch}/(W_{ch} \times t_{ch})$. In the fabricated 100 nm Cu_2O TFT, W_{ch} and t_{ch} are constant, and the S_{I_D} variable follows the ${L_{ch}}^{-1}$ dependence, indicating that the linear fitted gradient of L_{ch} versus S_{I_D} (10 Hz) is consistent with $m = -1$ in Figure 4D. The gradient of the 100 nm Cu_2O TFT corresponds to the dependence of R_{ch} and $S_{R_{ch}}$, as reported in previous studies. In the 30 nm Cu_2O TFT that presents a difference of approximately 0.3 times in t_{ch}, the change in the gradient of L_{ch} versus S_{I_D} corresponding to the t_{ch} change is observed in Figure 4D. According to our modified relational expression, the S_{R_T} variable of the 30 nm Cu_2O TFT follows a dependence of $3 \times {L_{ch}}^{-1}$, which demonstrates that the logarithmic calculated gradient is 0.5, which is consistent with the actual measurement value. The channel noise data were analyzed using the following formula to understand the physical origin of the slope:[24]

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$$\frac{S_{\mathrm{I,ch}}}{I_{\mathrm{D}}^{2}} = \frac{S_{\mathrm{I}}}{I_{\mathrm{D}}^{2}}\left(\frac{R_{\mathrm{T}}}{R_{\mathrm{T}} - R_{\mathrm{C}}}\right)^{2} \quad (4)$$

Figure 4E shows the slope of the channel-current PSD ($S_{\mathrm{I,ch}}/I_{\mathrm{D}}^{2}$) normalized to L_{ch} versus the drain current; the values extracted from the TLM method were used for R_{C}. The linear fitted slope in Figure 4E is similar to the slope of $S_{I_{\mathrm{D}}}/I_{\mathrm{D}}^{2}$ in the Cu_2O TFT, as shown in Figure 4D, indicating that the origin of the Cu_2O TFT noise depends upon t_{ch} as well as L_{ch} and W_{ch} of the Cu_2O thin films.

From the LFN results of the Cu_2O TFT, both the R_{ch} of the Cu_2O TFT and the R_{C} effect that occurred between the thin film and the Ni electrode were verified from the thermionic emission model through the Richardson plot, which is a type of Arrhenius plot, across a temperature range of 300 to 360 K. Panels A−C of Figure 5 present the Richardson plots of Cu_2O TFTs with t_{ch} of 30, 40, and 100 nm respectively, which are used to estimate the effective Richardson constant (A^*) and zero bias Schottky barrier height (Φ_{B}).[44,54−56] A^* of a 30, 40, and 100 nm Cu_2O TFT was estimated to be 0.00098, 0.00328, and 0.03246 A cm^{-2} K^{-2} from plot intercepts, respectively. The significantly lower values obtained when compared to the theoretical predictions indicate the impact of a smaller active area relative to the device area and the effects of barrier inhomogeneities. The quantified Φ_{B} is expressed as follows:

$$\Phi_{\mathrm{B}} = \frac{kT}{q}\ln\left(\frac{A_{\mathrm{d}}A^{*}T^{2}}{I_{\mathrm{D}}}\right) \quad (5)$$

where k is Boltzmann's constant, T is the absolute temperature, A_{d} is the channel region, and I_{D} is the drain current. The temperature versus Φ_{B} was investigated using Arrhenius plot for $1000/T$ in panels D−F of Figure 5.[55−57] The proportionality between t_{ch} and Φ_{B} was observed, but for the Cu_2O TFTs with the same t_{ch}, the influence of temperature on Φ_{B} is minimal. Similarly, our results indicate that the instabilities related to $1/f$ noise and thermal function increase within the device because R_{ch} is inversely proportional to the Cu_2O film thickness.

Figure 6 depicts the mobility degradation factors arising from the t_{ch} scaling of Cu_2O TFT. The Cu_2O TFTs with bulk conduction mechanisms were evaluated to increase the phonon/Coulomb scattering, Φ_{B}, and temperature instability in the bulk as the t_{ch} is scaled. In particular, the $1/f$ noise level incorporating these factors was verified to be associated with t_{ch}. Thus, maintaining a uniform film quality is crucial for preserving the mobility of Cu_2O TFTs, which are promising candidates for p-type semiconductors.

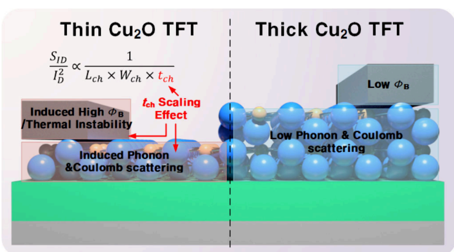

Figure 6. Schematic of the summarized noise-causing element by t_{ch} scaling of Cu_2O TFT.

■ CONCLUSION

In summary, we reported the $1/f$ noise behavior at low frequencies in Cu_2O TFTs and correlated the noise behavior with the reduced mobility owing to scattering inside the Cu_2O thin film. The $1/f$ noise behavior of the Cu_2O TFTs, whose thicknesses were adjusted through the PEALD process, is consistent with the HMF model commonly used for p-type semiconductors. The R_{ch} defined by the DC $I-V$ characteristics varied noticeably with the thickness change of the Cu_2O thin film when compared to R_{C}. The PSD behavior concerning L_{ch} and the difference t_{ch} of the Cu_2O TFTs was found to be opposite, and was dependent upon the PSD through the correlation of the channel components. Furthermore, temperature measurements reinforced the claim of mobility degradation with thickness dependence and the scattering mechanism in the thin film. Our results contribute significantly to the development of oxide semiconductor-based electronic devices and provide a better understanding of the mobility degradation mechanisms of p-type semiconductors and the random fluctuations occurring at low frequencies. In particular, the evaluation platform for PSD, which is inversely proportional to the proposed t_{ch} can be versatile when evaluating the noise in semiconductors with bulk conduction mechanisms.

■ EXPERIMENTAL METHODS

Device Fabrication. The Cu_2O TFT was fabricated in a bottom gate structure in which SiO_2 was grown to 90 nm through thermal growth and served as a gate dielectric layer. A p^{+}-doped silicon substrate served as the gate. The Cu_2O channel material was deposited on SiO_2 through the PEALD process.[25] Subsequently, the rapid thermal annealing (RTA) process was performed at 700 °C for 5 min in a N_2 atmosphere. The TLM pattern of the Cu_2O TFT was formed by UV exposure and 100 nm of Ni was deposited using an electron-beam evaporator. The Cu_2O thin films used in this study were deposited under similar conditions.

Device Characterization and Low-Frequency Noise Measurement. Five samples each with different thicknesses (30, 40, and 100 nm) were measured, and the average and standard error values for these values are represented as error bars. To prepare for unexpected effects when measuring the Cu_2O TFTs, measurements were performed using a Keithley 4200A-SCS parameter analyzer in a vacuum chamber at room temperature. The $C-V$ curve was measured using a Kesight E4980A Precision LCR meter. To collect the $1/f$ noise, we minimized external interference by connecting a suitable shared ground and shielding with a SR570 low-noise current preamplifier and an 89410A vector signal analyzer. The SR570 amplifies the input current to the output voltage and transmits the signal at 89410A. The 89410A was measured in units of 4 Hz from 10 to 1610 Hz, with 10 results derived from the average for a stable output. White noise was frequently observed above 1000 Hz and was omitted from the visualization.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.4c14876.

Additional TEM images of different thicknesses (Figure S2), EDS mapping images of the Cu_2O thin film (Figure S2), ToF-SIMS depth profile of the Cu_2O thin film (Figure S3), AFM analysis of Cu_2O thin films as-deposited and after PDA (Figure S4), TEM images of the Ni electrode and Cu_2O thin-film junction (Figure S5), UPS spectrum of the Cu_2O thin film (Figure S6), output and transfer curves of different thickness Cu_2O TFT (Figure S7), $S_{I_{\mathrm{D}}}$ versus frequency of the different thickness Cu_2O TFT (Figure S8), S_{I_D}/I_D^2 and corresponding CNF model as a function of the drain current for different thickness Cu_2O TFT (Figure S9), benchmark table of various p/n-type MOSFET Hooge parameters (Table S1), average and standard error of key parameters estimated from LFN results (Figure S10), results of transfer curves and LFN analysis of Cu_2O TFTs with Ti electrodes for high Schottky barrier (Figure S11), and resistance ratio curves of different V_G (Figure S12) (PDF)

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Notes

The authors declare no competing financial interest.

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